A REVIEW ON DESIGNING SUB THRESHOLD FLIP FLOPS FOR WIRELESS SENSOR NETWORK

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ABSTRACT

In a sensor node, maximum power is consumed by microcontroller since most of the functionalities are controlled or performed by it. Flip flop occupies major portion of microcontroller. Hence designing a low power flip flop cell is highly important forprolonging the life time of network. In this paper, we have reviewed and critically analyzed different sub threshold flip flop cells for wireless sensor networks.

Keywords: *Microcontroller, wireless sensor network, network lifetime, dynamic power management, dynamicpower dissipation, static power dissipation and D flip flops.*

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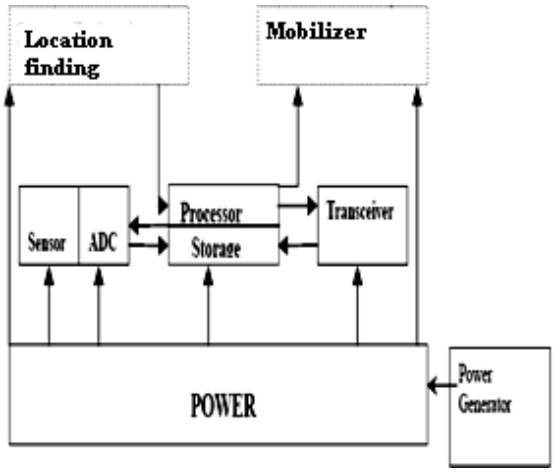
I. INTRODUCTION

Wireless sensor network (WSN) consists of low cost, low power distributed devices which is called sensor nodes. The role of each sensor node is to sense physical and environmental changes such as temperature, pressure etc. Each node has a limited communication range and storage capability.

Wireless sensor network is made up of four components: sensing unit, processing unit, transmission unit and power unit [1] as shown in Figure 1.

- Sensing unit: Sensing unit consist of sensor and analog to digital converters (ADCs). Sensor convert physical phenomenon to electrical signals. The analog signals produced by sensor are converted to digital signals by ADC and then fed to processing unit.
- Processing unit: Processing unit consists of microprocessor or microcontroller. This part of the node helps to control task scheduling, to calculate energy, to define communication protocols, to make suitable coordination and for data manipulation and data transfer.
- Transmission unit: Transmission unit receives the information from the CPU and then transmit it to the outside world.
- Power unit: The power supply unit is a crucial component of wireless sensor network. Battery power is the main source of energy. It supplies power to the complete sensor node, and hence plays a vital role in determining sensor node lifetime

Figure 1. Structural view of sensor network



Wireless sensor network find wide range of applications such as radiation level control, battlefield, noise pollution control, biological detection, structural health monitoring etc [2]. All sensors in the wireless sensor networks are battery operated which has limited power supply. Once the sensor nodes are deployed it is not possible to replace battery in the nodes. Therefore, optimal energy consumption by the nodes is necessary. Dynamic power management is one of the techniques to reduce power consumption. It shuts down the sensor node when there is no work and wakes up when required [3]. This yields better savings of energy and enhance lifetime.

Applications of WSNs

Applications of wireless sensor network are in -

- Building monitoring and control: Sensors embedded in a building can reduce energy cost by monitoring the temperature and lighting conditions in the buildings. In a ventilation system, sensor can be used to detect biological agents or chemical pollutants.
- Health care monitoring: The medical applications can be of two types: wearable and implanted. In wearable application devices are used on the surface of a human body or just at close proximity of the user. The implantable medical devices are those that are inserted inside human body.
- Industrial Monitoring: Using smart sensors, the condition of equipments in field and factories can be monitored to alert for imminent failures. This reduces cost for service and maintenance, increase machine up-time, improve customer satisfaction and even save lives.
- Agriculture: Wireless sensor network allows precise monitoring of crops at the time of its growth so that farmer can immediately know the state of the item at all its stages which will ease the decision process regarding the time of harvest [4].
- Smart Home Monitoring: Wireless sensors embedded within everyday objects forming a wireless sensor network is used to monitor the activities performed in a smart home.
- Environmental Monitoring: Sensors can be used for: air quality monitoring, air pollution monitoring, forest fire detection, landslide detection, water quality monitoring and so on. Sensors can also monitor biological or chemical hazards to provide early warnings.

2. RELATED WORK

Complementary Metal-Oxide-Semiconductor (CMOS) is the technology for designing integrated circuits that employ logic using both n- and p-channel MOSFET's. CMOS is the major technology utilized in manufacturing digital IC's and is now widely used in microprocessors, memories, and digital ASIC's. The low input currents required by a CMOS circuit results in lower power consumption, which is the major advantage of CMOS.

The total power dissipation of a circuit can be expressed as the sum of the static and the dynamic power dissipation component [5]. The dynamic power dissipation occurs due to charging and discharging of load capacitances and can be approximated as:

$$P_{dyn} = 1/2 \cdot \alpha \cdot C_L \cdot V_{DD}^2 \cdot f$$

where, α is the probability of a signal transition within a clock period, CL is the circuit capacitance to switch, VDD is the power supply voltage and f is the clock frequency.

From this equation, it can be observed that the dynamic power dissipation depends quadratically on the power supply voltage. Hence, reducing VDD is an effective way to reduce the dynamic power dissipation. Static power dissipation occurs due to non-ideal secondary CMOS effects such as subthreshold leakage current and other leakage currents in the transistor. Assuming a constant leakage current, the static power dissipation is given as [6]:

$P_{static} = I_{static} \cdot V_{DD}$

Subthreshold leakage current for $V_{gs} < V_{tn}$ for an n-type MOS transistor is given by:

$$I_{ds} = I_0 e^{(1-\kappa)V_{bs}/V_t} e^{\kappa V_{gs}/V_t}(1 - e^{-V_{ds}/V_t} + V_{ds}/V_0)$$

where,

V_{gs} is the gate-to-source voltage

V_{ds} is the drain-tosource voltage

V_{bs} is the substrate-to-source voltage (known as the body effect)

I_0 is the zero-bias current for the given device

V_t is the temperature voltage

$V_t = kT/q$
V_0 is the early voltage, κ is the effectiveness of the gate potential in controlling the channel current.

By reducing the supply voltage, and thus also Vgs, below the threshold voltage, the transistor channel is never fully inverted, but operates in weak or moderate inversion when the transistor is in 'on' state. For a n-type MOS transistor, weak inversion occurs when Vgs is approximately 100mV or more below the threshold voltage Vtn, and strong inversion occurs when Vgs is 100mV or more above Vtn. The region between weak and strong inversion is called moderate inversion

3. PROPOSED WORK

Flip flop is a major kind of sequential logic which plays an important role in modern synchronous digital circuits. In this section, we have discussed different sub threshold flip flop cells for wireless sensor networks.

A. C2MOS D flip flop

C2MOS stands for clocked CMOS and is an inverter-based master-slave D flip flop (DFF) which uses clocked inverters to control the loading of a new value, and to break the feedback loop. It is based on using two clocked inverter-based D-latches. The schematic for the C2MOS is shown in Figure 2.

In [7], this flip flop was proposed and simulated with a power supply voltage ranging from 350mV to 150mV at an operating frequency of 1MHz. The simulation result shows a delay time of 129.6ns and power dissipation of 350pW.So this
D flip flop cell was resized and modified [9] to reduce work voltage as shown in Figure 3. The VDDmin of improved C2MOS reduced from 230mV to 180mV.

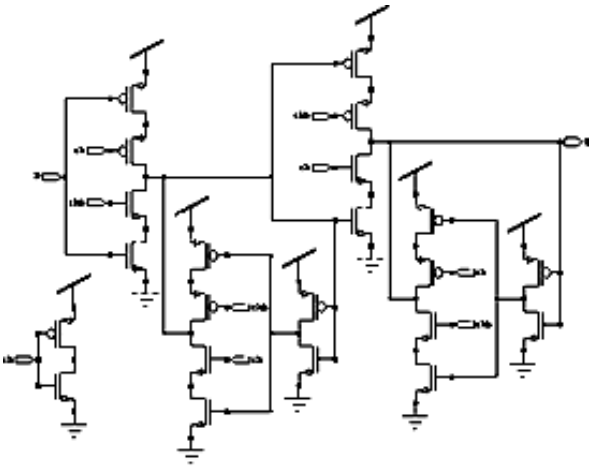


Figure 2.C^{2}MOS D flip flop

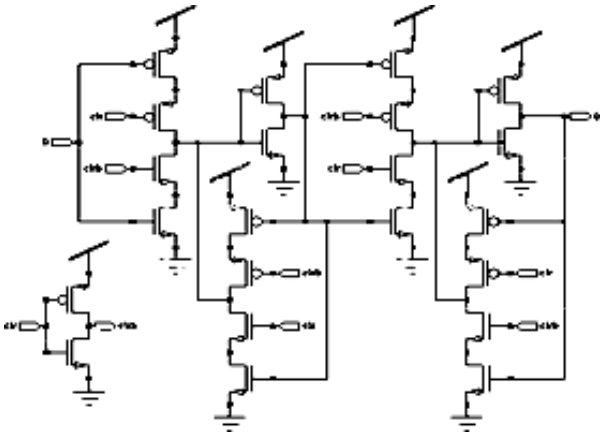


Figure 3.modified C^{2}MOS D flip flop

B. Transmission-gate Master-Slave (TGMS) flip-flop

The TGMS flip-flop is composed of two transmission gate-based latches operating on complementary clocks. This flip flop may be sensitive to clock-skew of its two complementary clock- phases as shown in Figure 4.

This flip flop was proposed and simulation was carried out with power supply voltage ranging from 350mV to 150mV and operating frequency of 1 MHz [7]. The simulation result shows a delay time of 129.8ns and power dissipation of 332.7pW. Hence, it was resized and modified to reduce work voltage [9]. The VDDmin of improved TGMS reduced from 230mV to 190mV.

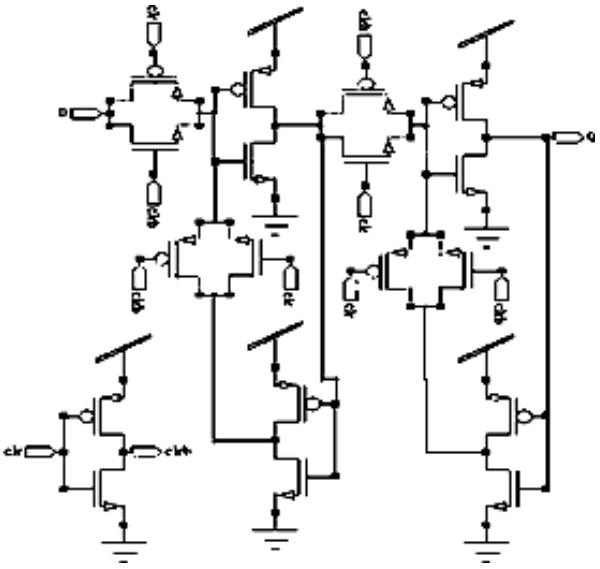


Figure 4. Transmission-gate Master-Slave (TGMS) flip-flop

C. PowerPC 603

This flip-flop is a combination of the TGMS and C2MOS flip-flops, using clocked inverters instead of feedback transmission gates as shown in Figure 5. It was used in the PowerPC 603 microprocessor data-path. For driving a high load, the static PowerPC 603 flip-flop shows the best overall performance, with a delay time of 16 ns and a power dissipation of 666 pW at 250mV. If the flip-flop is driving a lower load, the dynamic TGMS cell offers less delay and power dissipation, providing 20% lower delay time i.e. 119.7ns and 30% lower power dissipation i.e. 284.9pW compared to the PowerPC 603 flip-flop at VDD 250mV.

This flip flop cell was resized and simulated in 65nm and 90nm technology to reduce delay time and power dissipation [8]. In general, flip-flops in the 65 nm process show a lower delay time at the cost of higher power consumption compared to the same flip-flop designs in the 90 nm process. For sub-threshold operations, the PowerPC 603 has an increase in the EDP (energy delay product) value of 10 times in the 90 nm process compared to the 65 nm process. PowerPC 603 are structured by logics of inverters. So the inverter was redesigned so strong that it is functional under a lower supply voltage [9].

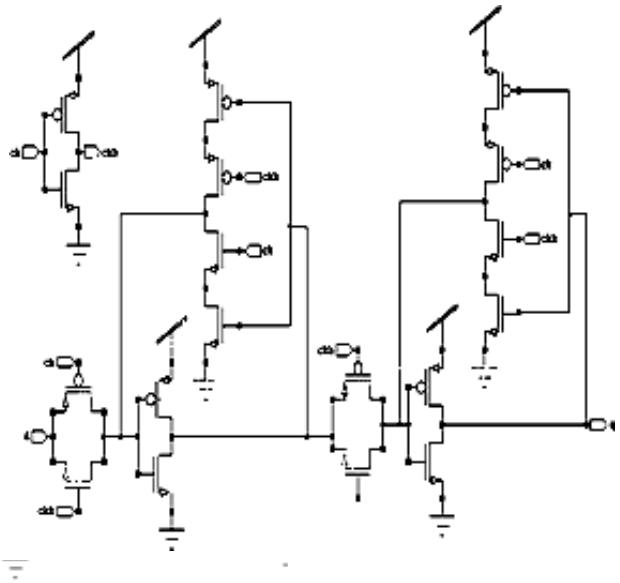


Figure 5.PowerPC 603

D. Sense Amplifier based D flip flop

The Sense-Amplifier based flip-flop (SAFF) consists of a sense-amplifier and S-R latch for capturing the output of the sense-amplifier as shown in Figure 6. With a power supply voltage ranging from 125mV to 1V this flip flop was simulated in 65nm and 90nm technology [8]. The simulation result shows a delay time of 19.6ns and power dissipation of 6.9nW in 65nm technology and delay time of 36.8ns and power dissipation of 1.5nW in 90nm technology. In [9] DFF cell was resized and modified to reduce work voltage.

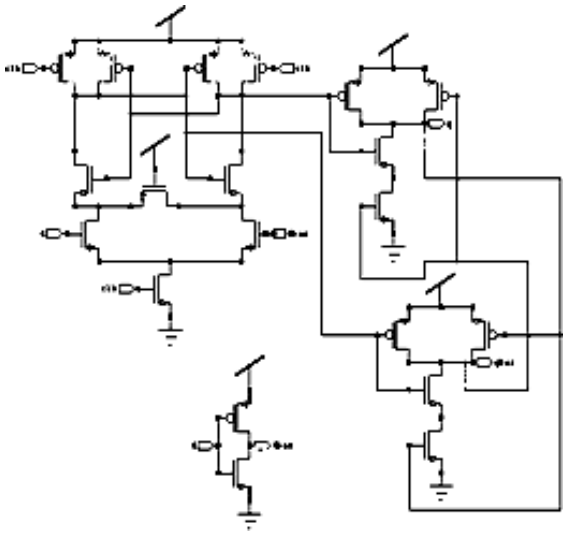


Figure 6.Sense Amplifier based D flip flop (SAFF)

CONCLUSION

In this paper, some widely used D flip flop cells are analyzed in sub threshold region. It is seen that PowerPC 603 flip flop cell offers best delay time and power dissipation of 120ns and 285pW respectively at supply voltage of 150mV. Low power dissipation is important in some low power applications and lowering supply voltage is the most effective way of decreasing power consumption. This comes at the cost of performance.

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